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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,154	08/29/2001	Michael L. Ziegler	10001163-1	6815

7590 05/28/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,154	ZIEGLER, MICHAEL L.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Chi (US Patent No. 5,701,435).

Chi discloses a computing arrangement comprising:

a processor (figure 1, 11) configured to execute a program;

a cache memory (12) coupled to the processor,

a system memory (13) coupled to the cache memory, wherein the processor is configured to execute an instruction that references data in the system memory and that specifies an alternate control path in the program (figures 2 and 3, see also col 1, lines 61 – 67);

means for determining whether the data referenced in the instruction are present in the cache memory (this is a necessary feature of a cache, see col. 1, lines 26 – 30, a cache miss results in the use of some bus cycles to acquire the referenced data); and

means for changing control flow of the program in accordance with the specified alternate control path if the referenced data are not present in the cache memory (col. 3, lines 3 – 8, branch instructions alter the execution sequence regardless of whether the reference data is present in the cache memory, i.e. cache hit, or not , i.e. cache miss).

3. With respect to claims 2, 5 and 6, the method further comprises:

returning the data referenced in the instruction from the cache memory to the processor if the referenced data are present in the cache memory; and

returning the data referenced in the instruction from the system memory to the processor if the referenced data are not present in the cache memory (col. 1, lines 13 – 23, and figure 1, this limitation describes a regular caching operation which is suggested by the figure along with the cited paragraphs).

4. With respect to claims 3, 8, 11 and 13, changing control flow further comprises branching to a program address specified by the instruction (col. 3, lines 3 – 8, also see figure 2).

5. With respect to claims 4, 9, 12 and 14, changing control flow further comprises skipping an instruction (col. 3, lines 3 – 8, when a conditional branch is executed, instructions it the path not taken are skipped).

6. With respect to claim 7, method further comprise if the referenced data are not present in the cache memory, bypassing loading of the data referenced in the instruction from the system memory to the cache memory (figure 1, cache bypass line).

7. With respect to claim 10, the method further comprises:

if the data are present in the cache memory, bypassing loading of the referenced data from the cache memory to the processor,

if the data are not present in the cache memory, bypassing loading of the referenced data from the system memory to the cache memory (figure 1, cache bypass line).

8. Claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Horowitz *et al.* (Informing Memory Operations, Proceedings, 23rd Annual International Symposium of Computer Architecture, May 1996, hereinafter "Horowitz").

Horowitz discloses a computing arrangement (page 1, introduction) comprising:

a processor configured to execute a program;

a cache memory coupled to the processor,

a system memory coupled to the cache memory, wherein the processor is configured to execute an instruction that references data in the system memory and that specifies an alternate control path in the program;

means for determining whether the data referenced in the instruction are present in the cache memory; and

means for changing control flow of the program in accordance with the specified alternate control path if the referenced data are not present in the cache memory (page 2, Informing Memory Operations, and page 3, 2.2 Low-overhead Cache Miss Traps).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eickemeyer et al. (US Patent Pub. No. 2001/0054137, and US Patent No. 6,061,710), Matoba (US Patent No. 5,594,884), Ebcioglu et al (US Patent No. 5,721,854), Stoodley (US Patent Pub. No. 2002/0144060), Chapple (US Patent Pub. No. 2002/0172320), Dowling (US Patent No. 6,157,988), an Nuechterlein et al (US Patent No. 6,594,755) disclose other systems that change the flow of the program on a cache miss.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
May 26, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100